Unified Current-Source Control for Low-Power Current-Mode-Logic Bit-Serial Circuits

Shogo Kisara and Michitaka Kameyama
Graduate School of Information Sciences, Tohoku University
Aoba-yama 6-6-05, Sendai 980-8579, Japan
kisara@kameyama.ecei.tohoku.ac.jp, kameyama@ecei.tohoku.ac.jp

Abstract

This paper presents a low-power multiple-valued VLSI based on two current-source control techniques. The first technique is a current-source control based on valid data signal detection. The other technique is a current-source control such that current sources are turned off within a clock cycle after a logic operation completion signal is detected. In a multiple-valued reconfigurable VLSI, power consumption of a cell with the low-power technique is reduced to 49% in comparison with that of the cell without the low-power technique, when the operating frequency is 500MHz, and the utilization ratio of the cell is 25%.

1 Introduction

Power consumption of a CMOS VLSI is increased due to a leakage current and a high operating frequency [1]. Performance degradation due to complexity of interconnections is also a serious problem [2]. We introduce a Multiple-Valued Current-Mode Logic (MVCML) to solve the problems [3]-[5]. The advantage of the MVCML is that linear summation by wiring, and that lower-power consumption can be achieved at high frequency in comparison with CMOS implementation if valid input data frequently arrives.

However, power consumption of the MVCML becomes larger than that of a CMOS VLSI if valid input data does not frequently arrive, because a clock gating technique used in a CMOS VLSI cannot be applied to the MVCML due to a constant current flow in a differential-pair circuit (DPC) [6]. Moreover, if the interval between the time when the logic block output becomes stationary and the end of the clock cycle, power consumption of the MVCML also becomes larger than that of the CMOS VLSI.

To solve the above problems, this paper presents two current-source control techniques for a low-power MVCML.

The first technique is a current-source control based on valid data signal detection. The valid data signal which indicates a word interval can be generated simply by using start/end signals in a bit-serial architecture. Using the valid data signal, current sources are controlled to be turned on or off. Start/end signals are always provided for each input/output data of a cell, so that simpler and lower-power current control scheme can be realized than the previously reported method [7]. The effect of the low-power technique depends on the utilization ratio of arithmetic and logic operations.

The other technique is a current-source control such that current sources are turned off within a clock cycle after a logic operation completion signal is detected. In the DPC, the logic operation completion signal can be generated by simple additional circuits. Moreover, a delay element is not necessary to keep sufficient turn-on time in the proposed method, which reduces delay and complexity of the control circuit [8]. This current-source control technique is especially effective at low frequency, because a current-source turn-off interval is increased.

Current sources are turned off in either of the following two conditions: One condition is that the valid data signal indicates ‘invalid’. The other is that the valid data signal indicates ‘valid’, and the logic operation completion signal is detected. Thus, these two techniques can be merged together.

In a multiple-valued reconfigurable VLSI based on the bit-serial architecture, power consumption of a cell with the low-power technique is reduced to 49% in comparison with that of the cell without the low-power technique, when the operating frequency is 500MHz, and the utilization ratio of the cell is 25%.
2 Multiple-valued VLSI based on bit-serial architecture

2.1 Superposition of bit-serial data and start/end signals

In the MVCML, the number of interconnections can be reduced by superposition of bit-serial data and start/end signals. If there are three data inputs, four interconnections are required for bit-serial operations in the binary VLSI as shown in Fig. 1, because an interconnection is necessary for start/end control in addition to three data inputs. On the other hand, in the MVCML, superposition of bit-serial data and start/end signals can be realized just by wiring, so that the number of interconnections can be half in comparison with the binary VLSI as shown in Fig. 2.

A Low-power technique is especially effective for a bit-serial architecture [9], because the number of warming-up clock cycles is relatively smaller for the total one-word clock cycle in the bit-serial architecture as shown in Fig. 3. While, the number of warming-up clock cycles is relatively larger for the total one-word clock cycle in the bit-parallel architecture.

2.2 Architecture of the multiple-valued VLSI

As an example of a basic design of an arithmetic and logic block based on the bit-serial architecture without a low-power technique, Fig. 4 shows a cell in the multiple-valued reconfigurable VLSI [10], [11].

As shown in Fig. 2, a three-valued input currents Ia and Ib are produced by superposition of two bit-serial data signals, and bit-serial data and start/end signals, respectively. The currents Ia and Ib are converted into three-valued voltages Va and Vb by an I-V convertor composed of pMOS transistors, respectively.

A start/end signal detector can be composed of a CMOS NOT circuit easily. Because the bit-serial data and start/end signals are, respectively, represented by “0,1” and “2”, the start/end signal can be extracted by a CMOS NOT circuit whose gate threshold is the voltage corresponding to “1.5”.

---

**Figure 1. Interconnections in the binary VLSI**

**Figure 2. Interconnections in the MVCML**

**Figure 3. Warming-up clock cycles**

**Figure 4. Basic design of a cell**
In an output generator, multiple-valued current signals are generated by superposition of the binary current output and start/end signals.

3 Current-source control for low-power operation

3.1 A Differential-pair circuit with current-source control capability

Figure 5 shows a DPC with current-source control capability. To control a current-source, a current-source control signal is used as input of the gate of pMOS transistors in the DPC. The current-source in the DPC is turned on when the current-source control signal is “0”, and turned off when the current-source control signal is “1”.

For an example, a logic circuit with current-source control capability can be constructed by cascade connection of two DPCs shown in Fig. 6. Turning off a current-source of a first DPC, complementary voltage inputs of a second DPC become 0V, so that the current-source of the second DPC can be turned off at the same time. The signal “control_out” is used to control the current sources of the succeeding DPCs. After the current-source of the first stage DPC is turned off in a logic circuit constructed by cascade connection of multiple DPCs, all the other current sources can be successively turned off.

3.2 Current-source control based on detection of an input data arrival

Power consumption of the MVCML becomes larger than a CMOS VLSI if valid input data does not frequently arrive, because a clock gating technique used in a CMOS VLSI cannot be applied to the MVCML due to the constant current flow. To solve the problem, current-source control technique by detecting a valid data signal shown in Fig. 7 is effective. The valid data signal can be generated by a control circuit C1 shown Fig.8 constructed by the start/end signal detector, and a T flip-flop (T-FF) whose present output is inverted at every rising edge, and a D-FF. The valid data signal becomes “1”, and current sources are turned on when the start signal is detected. On the other hand, the valid data signal becomes “0”, and current sources are turned off when
the end signal is detected.

The valid data signal is generated by using the start/end signal one clock before the data arrival. Let the valid data signal be generated in the delay time $t_1$, and let the delay time of a one-bit logic operation be $t_2$. Accordingly, one clock cycle is determined by $t_2$ in the case of $t_2 \geq t_1$. On the other hand, if the valid data signal is generated, and the first-bit logic operation is done within one clock cycle, then one clock cycle is determined by $t_1 + t_2$. Therefore, an operation time of one word can be greatly reduced.

As an example of the arithmetic and logic block designed based on the current-source control technique, Fig. 9 shows a cell in the multiple-valued reconfigurable VLSI. An additional circuit of C1 enclosed by the broken line is included as shown in Fig. 9.

3.3 Current-source control based on logic operation completion within a clock cycle

If the interval between the time when the logic block output becomes stationary and the end of the clock cycle, power consumption of the MVCML becomes larger than that of the CMOS VLSI is large. To solve the problem, a current-source control such that current sources are turned off within a clock cycle after a logic operation completion signal is detected shown in Fig. 10 is effectively employed.

A control circuit C2 which generates a current-source control signal within a clock cycle is designed using CMOS gates as shown in Fig. 11.

When the logic operation is completed, the logic operation completion signal becomes “0” which turns off current sources. Otherwise, the logic operation completion signal remains “1”. The logic operation completion signal can be generated simply by additional circuits shown in Fig. 12.

As an example of the arithmetic and logic block designed based on this current-source control technique, Fig. 13 shows a cell in the multiple-valued reconfigurable VLSI. The current-source control signal is used to control not only current-source in the logic block, but also input data. The input timing can be synchronous with the turn-on timing in the DPC, and power consumption can be reduced by controlling input data.

An RS flip-flop is used to store the logic operation completion result in a register, because arrival of correct values of R and S is assured immediately before both R and S become “0”.

Figure 9. Cell designed based on the current-source control technique

Figure 10. Current-source control technique by logic operation completion detection

Figure 11. Control circuit C2

Figure 12. Logic operation completion signal
3.4 Integration of two kinds of the current-source control circuits

Two current-source control techniques based on detection of the valid input data arrival and the logic operation completion within a clock cycle are proposed. These two techniques can be merged together to achieve low-power operations. The current-source control using the valid data and logic operation completion signals is effectively done as shown in Fig. 14.

When the valid data signal indicates ‘invalid’ in the arithmetic and logic block designed based on two current-source control techniques, power consumption of the CMOS control circuit C2 can be reduced just by making the logic operation completion signal “0” which becomes an input value of C2. If the DPC current sources are turned off, the logic operation completion signal becomes “0”, because its complementary outputs cannot be generated. Therefore, power consumption of the CMOS control circuit C2 can be reduced just by making the current control signal “1” when the valid data signal indicates ‘invalid’.

As an example of the arithmetic and logic block designed based on two current-source control technique, Fig. 15 shows a cell in the multiple-valued reconfigurable VLSI.

4 Evaluation

A 8-bit full-adder function is programmed in the cell of the multiple-valued reconfigurable VLSI shown in Fig. 15. The performance evaluation of the cell with proposed low-power technique is done based on HSPICE simulation using a 65nm CMOS design rule. The performance of the cell
with proposed low-power technique is compared with that of the cell without low-power technique.

Figure 16 shows power consumption versus the proportion of the valid data arrival which corresponds to the utilization ratio of the cell when the operating frequency is 500MHz. Power consumption of the cell is dependent on the utilization ratio by the current-source control technique based on detection of the input data arrival. For example, Power consumption of the cell with low-power technique is reduced to 49% than that of the cell without current-source control technique when the operating frequency is 500MHz, and the utilization ratio of the cell is 25%.

Figure 17 shows power consumption versus the operating frequency of the cell when the utilization ratio of the cell is 50%. It is evaluated that the reduction of the power consumption is remarkable, if the operating frequency is less than 920MHz. The number of transistors in the cell and the delay time of a one-bit logic operation are evaluated as shown in Table 1.

5 Conclusion

Two current-source control techniques are proposed based on superposition of bit-serial data and current-source control signals. The VLSI with two current-source control techniques is especially effective for the reduction of power consumption when the utilization ratio and the operating frequency are low.

As a future problem, we need to obtain the most appropriate granularity of the proposed current-source control technique from the view point of minimization of the total power consumption considering that of the control circuits.

References